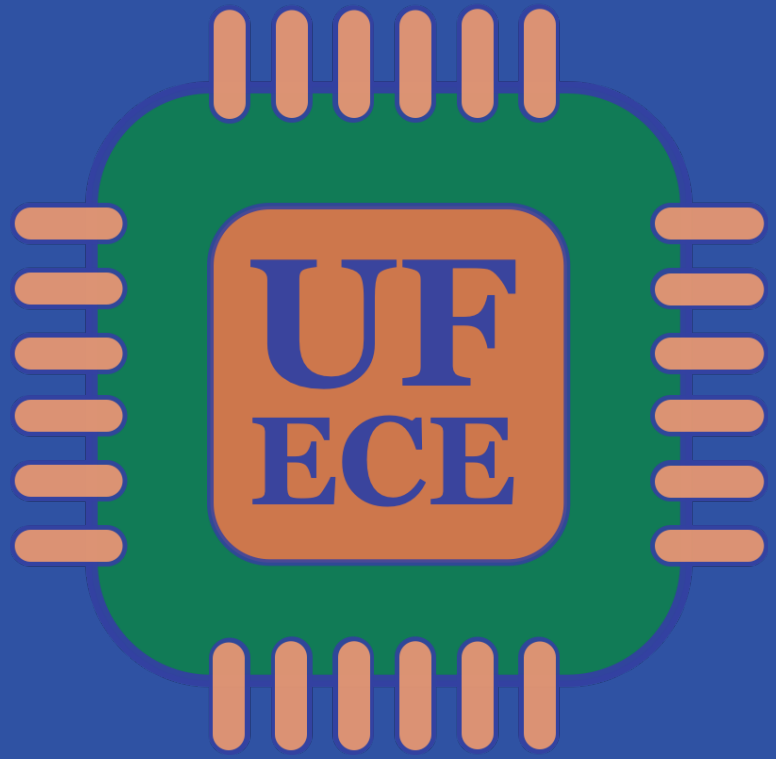
# Microprocessor Applications

## *XMEGA: DAC*

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# XMEGA DAC Specifications

The XMEGA has two digital-to-analog converter (**DAC**) modules, one on Port A and the other on Port B. Each module has two channels that can operate separately.

- Each channel within a DAC module has its own designated output pin:
  - **DAC0**: DAC channel 0 output
  - **DAC1**: DAC channel 1 output
- 12-bit resolution
- Up to 1 mega-samples per second (1 MSPS) conversion rate

- The naming convention for labeling each individual module is DAC*p*, where *p* specifies the port:
  - *p* : {A, B}
  - For example, **Port A** has a DAC module labeled **DACA**.

# Alternate Pin Function Table

- Section 33.2 of doc8385 has a table of alternate pin functions for each port.
- The table for Port A is shown here. See the column labeled "DACA." Port B is similar.

| PORTA | PIN # | INTERRUPT | ADCA POS /GAINPOS | ADCB POS | ADCA NEG | ADCA GAINNEG | ACA POS | ACA NEG | ACA OUT | DACA | REFA |
|---|---|---|---|---|---|---|---|---|---|---|---|
| GND | 93 | | | | | | | | | | |
| AVCC | 94 | | | | | | | | | | |
| PA0 | 95 | SYNC | ADC0 | ADC8 | ADC0 | | AC0 | AC0 | | | AREF |
| PA1 | 96 | SYNC | ADC1 | ADC9 | ADC1 | | AC1 | AC1 | | | |
| PA2 | 97 | SYNC/ASYNC | ADC2 | ADC10 | ADC2 | | AC2 | | | DAC0 | |
| PA3 | 98 | SYNC | ADC3 | ADC11 | ADC3 | | AC3 | AC3 | | DAC1 | |
| PA4 | 99 | SYNC | ADC4 | ADC12 | | ADC4 | AC4 | | | | |
| PA5 | 100 | SYNC | ADC5 | ADC13 | | ADC5 | AC5 | AC5 | | | |
| PA6 | 1 | SYNC | ADC6 | ADC14 | | ADC6 | AC6 | | AC1OUT | | |
| PA7 | 2 | SYNC | ADC7 | ADC15 | | ADC7 | | AC7 | AC0OUT | | |

doc8385 Table 33-1

# Block Diagram

Here is the block diagram for a DAC module.

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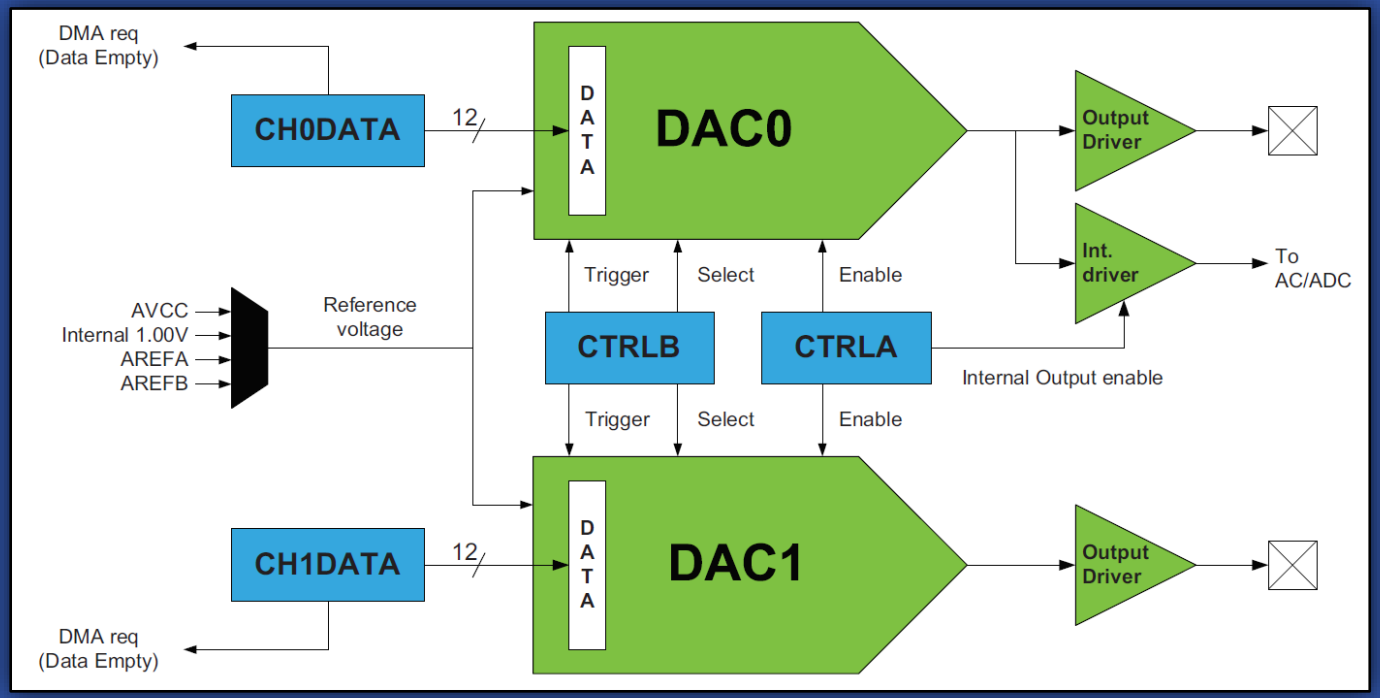
Figure 29-1

- Each DAC channel, if enabled, performs a new conversion (outputs a new voltage value) when either of the following occur:
  - Data is written its data register
  - A trigger from the Event System
- Several options for reference voltages exist.



# DAC Initialization Procedure

The recommended order of initializations for a DAC module is as follows:

1) Choose single- or dual-channel operation. (CTRLB)
2) Select channel(s) to be triggered by events, if applicable. (CTRLB)
3) Select a reference voltage and decide if the data is supplied left- or right-adjusted. (CTRLC)
4) Enable the channel(s) to be utilized. (CTRLA)
5) Enable the entire DAC module. (CTRLA)

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4) Enable the channel(s) to be utilized. (CTRLA)
5) Enable the entire DAC module. (CTRLA)

# Initialization – Channel Selection

- The Channel Selection (**CHSEL[1:0]**) bitfield determines which DAC channels are to be utilized.
  - For single-channel operation, either channel 0 or 1 can be used.
  - For dual-channel operation, both channels 0 and 1 are used.

| CHSEL[1:0] | Group configuration | Description |
|---|---|---|
| 00 | SINGLE | Single-channel operation on channel 0 |
| 01 | SINGLE1 | Single-channel operation on channel 1 |
| 10 | DUAL | Dual-channel operation |
| 11 | – | Reserved |

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Table 29-1

CTRLB

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| – | CHSEL[1:0] | | – | – | – | CH1TRIG | CH0TRIG |

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Section 29.10.2

# DAC Initialization Procedure

The recommended order of initializations for a DAC module is as follows:

1) ~~Choose single- or dual-channel operation. (CTRLB)~~
2) Select channel(s) to be triggered by events, if applicable. (CTRLB)
3) Select a reference voltage and decide if the data is supplied left- or right-adjusted. (CTRLC)
4) Enable the channel(s) to be utilized. (CTRLA)
5) Enable the entire DAC module. (CTRLA)

# Initialization – Enable Event System Trigger(s)

- The **CH1TRIG** and **CH0TRIG** bits enable an event from the Event System to trigger a conversion on channel 1 or 0, respectively.
  - If enabled, the event channel that triggers each channel must be configured using the DAC module's EVCTRL register.

CTRLB

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| – | CHSEL[1:0] | | – | – | – | CH1TRIG | CH0TRIG |

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Section 29.10.2

# DAC Initialization Procedure

The recommended order of initializations for a DAC module is as follows:

1) ~~Choose single- or dual-channel operation. (CTRLB)~~
2) ~~Select channel(s) to be triggered by events, if applicable. (CTRLB)~~
3) Select a reference voltage and decide if the data is supplied left- or right-adjusted. (CTRLC)
4) Enable the channel(s) to be utilized. (CTRLA)
5) Enable the entire DAC module. (CTRLA)

# Initialization – Reference Voltage Selection

- The **REFSEL[1:0]** bitfield determines which reference voltage source is used.
  - AREFA and AREFB can be applied externally on pin 0 of Port A and B, respectively.

| CHSEL[1:0] | Group configuration | Description |
|---|---|---|
| 00 | INT1V | Internal 1.00V |
| 01 | AVCC | $AV_{CC}$ |
| 10 | AREFA | AREF on PORTA |
| 11 | AREFB | AREF on PORTB |

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Table 29-2

CTRLC

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| – | – | – | REFSEL[1:0] | | – | – | LEFTADJ |

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# Initialization – Left- or Right-Justification

- The **LEFTADJ** bit determines whether the input data is to be interpreted as left-adjusted or right-adjusted:
  - When LEFTADJ = 1, input data is interpreted as left-adjusted.
  - When LEFTADJ = 0, input data is interpreted as right-adjusted.
- Note that this configuration applies to BOTH channels.
- More details regarding when to choose each justification will be provided later in the slides that cover the channel DATA registers.

CTRLC

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| – | – | – | REFSEL[1:0] | | – | – | LEFTADJ |

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Section 29.10.3

# DAC Initialization Procedure

The recommended order of initializations for a DAC module is as follows:

1) ~~Choose single- or dual-channel operation. (CTRLB)~~
2) ~~Select channel(s) to be triggered by events, if applicable. (CTRLB)~~
3) ~~Select a reference voltage and decide if the data is supplied left- or right-adjusted. (CTRLC)~~
4) Enable the channel(s) to be utilized. (CTRLA)
5) Enable the entire DAC module. (CTRLA)

# Initialization – Enable Channel(s)

- The **CH1EN** and **CH0EN** bits, when set, individually make each channel's analog output available on its output pin.

CTRLA

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| – | – | – | IDOEN | CH1EN | CH0EN | LPMODE | ENABLE |

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Section 29.10.1

# DAC Initialization Procedure

The recommended order of initializations for a DAC module is as follows:

1) ~~Choose single- or dual-channel operation. (CTRLB)~~
2) ~~Select channel(s) to be triggered by events, if applicable. (CTRLB)~~
3) ~~Select a reference voltage and decide if the data is supplied left- or right-adjusted. (CTRLC)~~
4) ~~Enable the channel(s) to be utilized. (CTRLA)~~
5) Enable the entire DAC module. (CTRLA)

# Initialization – Enable DAC Module

- The **ENABLE** bit, when set, enables the entire DAC module.

CTRLA

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| – | – | – | IDOEN | CH1EN | CH0EN | LPMODE | ENABLE |

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# Using the DAC – Data Registers

- The digital value to be converted by the DAC is supplied via the 16-bit CH*n*DATA register, where $n = 0, 1$.
  - Each channel's DATA register is comprised of two 8-bit registers: CH*n*DATAH and CH*n*DATAL.

## CH*n*DATAL

| | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| Right-adjust | +0x18 | CHDATA[7:0] | | | | | | | |
| Left-adjust | | CHDATA[3:0] | | | | – | – | – | – |

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## CH*n*DATAH

| | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| Right-adjust | +0x19 | – | – | – | – | CHDATA[11:8] | | | |
| Left-adjust | | CHDATA[11:4] | | | | | | | |

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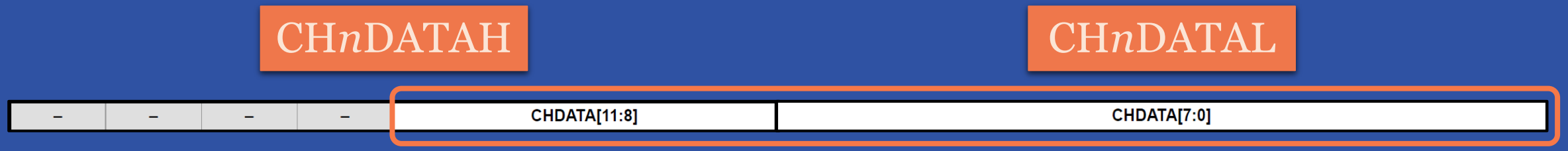
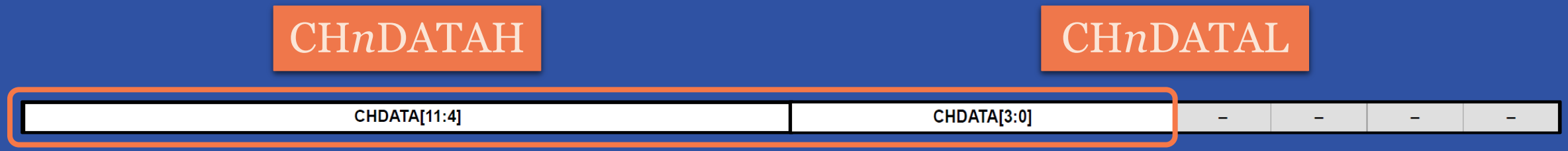
# Using the DAC – Right- vs. Left-Adjusted Data

- Whenever **LEFTADJ** = 0 within the CTRLC register, which is the default value, the CH*n*DATA register is interpreted as right-adjusted.




- Whenever **LEFTADJ** = 1, the CH*n*DATA register is interpreted as left-adjusted.



# Using the DAC – Before Writing to the CH*n*DATA Register

- Before manually writing data to the DATA register(s), the **CH1DRE** and **CH0DRE** bits should be polled to verify there is not already a pending conversion.
- When one of these bits is set, the respective channel's data register is empty.
  - This indicates that it is safe to write data without overwriting a pending conversion.

STATUS

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| – | – | – | – | – | – | CH1DRE | CH0DRE |

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# Using the DAC – Writing to the CH*n*DATA Register

- During standard operation, when events are not utilized, writing to the CH*n*DATA register starts a conversion.
- The low byte of this register (CH*n*DATAL) must be written to first, followed by the high byte (CH*n*DATAH), because writing to the high byte is what initiates the conversion.
- The DAC can do **8-bit conversions** by using left-adjusted data, which allows data to be exclusively written to the CH*n*DATAH register.
  - Doing 8-bit conversions like this saves some execution time by reducing the number of writes required to perform a conversion, but because only eight bits are being utilized, the resolution is decreased.

CH*n*DATAH

| – | – | – | – | CHDATA[11:8] |
|---|---|---|---|---|
| CHDATA[11:4] | | | | |

CH*n*DATAL

| CHDATA[7:0] | | | | | | | |
|---|---|---|---|---|---|---|---|
| CHDATA[3:0] | | | | – | – | – | – |

# Conclusion

- The XMEGA's DAC system is relatively easy to setup and get working quickly.
- The DAC and ADC systems can be used together.
- Section 29 of the XMEGA AU manual (doc8331) contains all the details that you may need to learn regarding the DAC system.